APPENDIX B

"Marked Up" paragraphs showing the changes that the accompanying submission makes to the specification of Serial No. 09/931,229:

Please replace the paragraph beginning on Page 8, line 13 with the following amended paragraph:

Also connected to pad 20, and therefore to B^+, is a serpentine conductor 30 that may, as are pads 20 and 21, be printed on the top surface of PCB 100. As may be seen in Figure 2, serpentine conductor 30 comprises an originating segment 31 connected to pad 20 and a terminating segment 32 coupled to a planar conductor 40. (The relevance of conductor 40 will be revealed below.) Conductor 30 also comprises a number of substantially linear segments 34a, 34b, 34c, and 34d. Liner segment 34a is joined to originating segment 31 by a first turn 33a and is joined to linear segment 34b by a second turn 33b. Linear segment 34b is joined to linear segment 34c by a third turn 33c, and linear segment 34c is joined to linear segment 34d by a fourth turn 33d. The serpentine conductor is terminated, at terminating segment 32, in the substantially rectangular, [planar pad] conductor 40 formed as a planar pad.

Please replace the paragraph beginning on Page 9, line 5 with the following amended paragraph:

In an exemplary embodiment, tuning capacitance conductor 40 may be configured in rectangular form, as depicted in Figure 2. However, those skilled in the art will recognize that tuning capacitance conductor 40 may assume other geometries, including square, circular, triangular, etc. and may adopt an irregular shape. However, in order for conductor 40 to instantiate a capacitance at F_o, conductor 40 must subtend an appropriate area on the PCB and must be positioned in some proximity to a second conductor. In the arrangement of Figure 2, conductor 40 as positioned to be proximate a ground plane 60. In one embodiment (Figure 2A), conductor 40 may be deposited on the top surface of the PCB, diametrically opposed a ground plane that is deposited on the bottom surface. In this configuration, the tuning capacitance is formed by conductor 40, ground plane 60, and intervening (between conductor 40 and ground

plane 60) thickness of the dielectric PCB 100. In an alternative, but perhaps less effective embodiment (Figure 2B), ground plane 60 may envelop portions of conductor 40 on the top surface of PCB 100. The essence is that conductor 40 is to form one "plate" of a capacitor, and the ground plane on system board forms the second "plate." In this manner, serpentine conductor 30 and conductor 40 effectively form a series LC network, at F_0, between pad 20 and GND. Note, however, that there exists no electrical continuity by virtue of LC network between pad 20 and GND.

Please replace the paragraph beginning on Page 10, line 1 with the following amended paragraph:

For example, in a situation in which 400 MHz noise must be prevented or blocked from appearing at the B^+ pin of an ASIC on the system board, where, for example, a discrete 0.01 uf bypass capacitor as deployed, a simulation effort was conducted to determine the corresponding geometries of the printed circuit inductor 30 and printed circuit capacitor conductor 40 to realize series resonance at 400 MHz. In order to trade inductor to resonant at 400 MHz, simulation indicated that a 2.7 inches trace length (L), 5 mils trace width (W), 5 mils trace space (S), and three turns (N). The tuning capacitor was formed as a square, approximately 135 mils x 135 mils. When the serpentine trace resonants at 400 MHz, a low impedance path from the discrete capacitor's power pad to the ground plane (under the serpentine trace on the board) is effected, and the 400 MHz noise is substantially attenuated.

Please replace the paragraph beginning on Page 11, line 1 with the following amended paragraph:

The Detailed Description, insofar as provided above, has elaborated a specific embodiment of the invention in generous detail, so as to enable a skilled artisan to understand and exploit the invention. However, certain ramifications of the invention are worthy of elaboration. In particular, the LC network has been described as including an inductance 30 and a tuning capacitance conductor 40. To be rigorously precise, as distributed circuit elements, there is both a quantum of capacitance associated with conductor 30 and a quantum of inductance associated with conductor 40. However, at a frequency of interest, F_o, conductor 30 is predominantly inductive and conductor 40 is predominantly capacitive. In this regard

(inductive) conductor 30 is particularly described as having a serpentine geometry. However, the invention comprehends other geometries that, at a predetermined F_o, exhibit an inductive impedance. A serpentine conductor results in an inductance at high frequencies, in large part, because of the directional changes necessarily imparted to the current flowing through it. Similarly (capacitive) conductor 40 invites other geometries as well, and a rectangular perimeter is propounded largely for simplicity and regularity. Those skilled in the art realize that the resulting capacitance of conductor 40 is largely dependent on the area subtended by the conductor, the thickness of the PCB 101, and its dielectric properties.